

Case No.: DENSE-052A

CSP CHIP STACK WITH FLEX CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

(Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

(Not Applicable)

BACKGROUND OF THE INVENTION

**[0001]** The present invention relates generally to chip stacks, and more particularly to a chip stack having connections routed from the bottom to the perimeter thereof to allow multiple integrated circuit chips such as CSP devices to be quickly, easily and inexpensively vertically interconnected in a volumetrically efficient manner.

**[0002]** Multiple techniques are currently employed in the prior art to increase memory capacity on a printed circuit board. Such techniques include the use of larger memory chips, if available, and increasing the size of the circuit board for purposes of allowing the same to accommodate more memory devices or chips. In another technique, vertical plug-in boards are used to increase the height of the circuit board to allow the same to accommodate additional memory devices or chips.

**[0003]** Perhaps one of the most commonly used techniques to increase memory capacity is the stacking of memory devices into a vertical chip stack, sometimes referred to as 3D packaging or Z-Stacking. In the Z-Stacking process, as from two (2) to as many as eight (8) memory devices or

other integrated circuit (IC) chips are interconnected in a single component (i.e., chip stack) which is mountable to the "footprint" typically used for a single package device such as a packaged chip. The Z-Stacking process has been found to be volumetrically efficient, with packaged chips in TSOP (thin small outline package) or LCC (leadless chip carrier) form generally being considered to be the easiest to use in relation thereto. Though bare dies or chips may also be used in the Z-Stacking process, such use tends to make the stacking process more complex and not well suited to automation.

**[0004]** In the Z-Stacking process, the IC chips or packaged chips must, in addition to being formed into a stack, be electrically interconnected to each other in a desired manner. There is known in the prior art various different arrangements and techniques for electrically interconnecting the IC chips or packaged chips within a stack. Examples of such arrangements and techniques are disclosed in Applicant's U.S. Patent Nos. 4,956,694 entitled INTEGRATED CIRCUIT CHIP STACKING issued September 11, 1990, 5,612,570 entitled CHIP STACK AND METHOD OF MAKING SAME issued March 18, 1997, and 5,869,353 entitled MODULAR PANEL STACKING PROCESS issued February 9, 1999.

**[0005]** The various arrangements and techniques described in these issued patents and other currently pending patent applications of Applicant have been found to provide chip stacks which are relatively easy and inexpensive to manufacture, and are well suited for use in a multitude of differing applications. The present invention provides yet a further alternative arrangement and technique for forming a volumetrically efficient chip stack. In the chip stack of the present invention, connections are routed from the bottom of the chip stack to the perimeter thereof so that interconnections can be made vertically which allows

multiple integrated circuit chips such as BGA, CSP, fine pitch BGA, or flip chip devices to be stacked in a manner providing the potential for significant increases in the production rate of the chip stack and resultant reductions in the cost thereof.

BRIEF SUMMARY OF THE INVENTION

**[0006]** In accordance with one embodiment of the present invention, there is provided a chip stack comprising a flex circuit. The flex circuit itself comprises a flex substrate having a first conductive pattern disposed thereon, and a plurality of leads extending therefrom. The leads of the flex circuit are electrically connected to the first conductive pattern thereof. In addition to the flex circuit, the chip stack comprises at least two integrated circuit chip packages which are electrically connected to the first conductive pattern. The first conductive pattern comprises first and second sets of flex pads which are disposed on respective ones of the opposed top and bottom surfaces of the flex substrate, with one of the integrated circuit chip packages being disposed on the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set, and one of the integrated circuit chips being disposed upon the bottom surface of the flex substrate and electrically connected to at least some of the flex pads of the second set. The integrated circuit chip packages may each comprise a CSP device.

**[0007]** In accordance with another embodiment of the present invention, there is provided a chip stack comprising a flex circuit. The flex circuit itself comprises a flex substrate having a first conductive pattern disposed thereon, and a plurality of conductive leads extending therefrom. The leads of the flex circuit

are electrically connected to the first conductive pattern thereon. The chip stack further comprises at least two integrated circuit chip packages, one of which is electrically connected to the first conductive pattern, with the remaining integrated circuit chip package being in non-conductive attachment to the flex substrate. The first conductive pattern of the flex circuit comprises a first set of flex pads disposed on the top surface of the flex substrate and electrically connected to respective ones of the leads. One of the integrated circuit chip packages is disposed upon the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set, with the remaining integrated circuit chip package being attached to the bottom surface of the flex substrate. The conductive contacts of the integrated circuit chip package attached to the bottom surface of the flex substrate and the leads of the flex circuit collectively define a composite footprint of the chip stack which is electrically connectable to another component. The leads of the chip stack may each comprise either an S-lead or a J-lead.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0008]** These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

**[0009]** Figure 1 is a side-elevational view of a chip stack constructed in accordance with a first embodiment of the present invention;

**[0010]** Figure 2 is a top perspective view of the flex circuit included in the chip stack shown in Figure 1;

**[0011]** Figure 3 is a side-elevational view of a chip stack constructed in accordance with a second embodiment of

the present invention; and

**[0012]** Figure 4 is a side-elevational view of a chip stack constructed in accordance with a third embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0013]** Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figure 1 depicts a chip stack 10 constructed in accordance with a first embodiment of the present invention. Referring now to Figures 1 and 2, the chip stack 10 comprises a flex circuit 12. The flex circuit 12 itself comprises a rectangularly configured flex substrate 14 which defines a generally planar top surface 16, a generally planar bottom surface 18, an opposed pair of longitudinal peripheral edge segments 20, and an opposed pair of lateral peripheral edge segments 22.

**[0014]** Disposed on the flex substrate 14 of the flex circuit 12 is a first conductive pattern. The first conductive pattern itself preferably comprises a first set of flex pads 24 which are disposed on the top surface 16 of the flex substrate 14, and a second set of flex pads 25 which are disposed on the bottom surface 18 of the flex substrate 14. The flex pads 24 of the first set are arranged in a generally rectangular pattern or array in the central portion of the top surface 16. Likewise, the flex pads 25 of the second set are arranged in a generally rectangular pattern or array in the central portion of the bottom surface 18. It is contemplated that the flex pads 24 of the first set and the flex pads 25 of the second set will be arranged in identical patterns, with each of the flex pads 24 of the first set being coaxially aligned with a respective one of the flex pads 25 of the second set.

However, those of ordinary skill in the art will recognize that the flex pads 24 of the first set and the flex pads 25 of the second set may be disposed upon the flex substrate 14 in dissimilar patterns. Additionally, though the flex substrate 14 is described as being rectangularly configured, it will be recognized that the same may be formed in alternative shapes (e.g., square).

**[0015]** Extending from one or more of the longitudinal and lateral peripheral edge segments 20, 22 of the flex substrate 14 are a plurality of conductive leads 26. The leads 26 each comprise an S-lead (i.e., gull wing) having the general shape of the letter S. Each of the leads 26 are electrically connected to the first conductive pattern and, in particular, to the flex pads 24, 25 of the first and second sets. The first conductive pattern of the flex circuit 12 may be configured such that the flex pads 24 of the first set and the flex pads 25 of the second set are each electrically connected to respective ones of the leads 26. It is also contemplated that two or more flex pads 24 of the first set may be electrically connected to a single lead 26, and that two or more flex pads 25 of the second set may be electrically connected to a single lead 26. Still further, one or more flex pads 24 of the first set in combination with one or more flex pads 25 of the second set may be electrically connected to a single lead 26. In this regard, the first conductive pattern may include conductive traces which extend within the flex substrate 14 in any pattern or arrangement as is needed to achieve a desired signal routing. Any flex pad 24 of the first set may be electrically connected to the flex pad 25 of the second set coaxially aligned therewith by a via or feed-through hole extending through the flex substrate 14 therebetween.

**[0016]** In the chip stack 10, the flex pads 24 of the first set, the flex pads 25 of the second set, and the

conductive traces extending within the flex substrate 14 are each preferably fabricated from very thin copper having a thickness in the range of from about five microns to about twenty-five microns through the use of conventional etching techniques. The use of thin copper for the various pads and traces allows for etching line widths and spacings down to a pitch of about four mils which substantially increases the routing density of the flex circuit 12. The flex substrate 14 is preferably fabricated from either FR-4, a polyimide film, or some other suitable material which can easily be routed. The material used to form the flex substrate 14 may be as thin as about fifty microns or may be a thicker multi-layer structure.

**[0017]** The chip stack 10 further comprises at least two identically configured integrated circuit chip packages 28. Each of the integrated circuit chip packages 28 comprises a rectangularly configured package body 30 defining a generally planar top surface 32, a generally planar bottom surface 34, an opposed pair of longitudinal sides, and an opposed pair of lateral sides. Disposed on the bottom surface 34 of the package body 30 are a plurality of spherically or semi-spherically shaped conductive contacts 36 which are preferably arranged in a pattern identical to the patterns of the flex pads 24 of the first set and the flex pads 25 of the second set. The conductive contacts 36 of one of the integrated circuit chip packages 28 are electrically connected to respective ones of the flex pads 24 of the first set, with the conductive contacts 36 of the remaining integrated circuit chip package 28 being electrically connected to respective ones of the flex pads 25 of the second set. Such electrical connection is preferably accomplished via soldering. Each of the integrated circuit chip packages 28 is preferably a CSP (chip scale package) device such as a BGA (ball grid array)

device, a fine pitch BGA device, or a flip chip device.

**[0018]** In assembling the chip stack 10, the integrated circuit chip packages 28 are electrically connected to the first conductive pattern of the flex circuit 12 in the above-described manner. As further seen in Figure 1, a layer 38 of flux/underfill material may optionally be applied between the bottom surfaces 34 of the package bodies 30 and respective ones of the top and bottom surfaces 16, 18 of the flex substrate 14. The leads 26 are sized relative to the integrated circuit chip packages 28 such that the outwardly turned distal end of each lead 26 extends beyond the top surface 32 of the lowermost integrated circuit chip package 28 of the chip stack 10 (i.e., the integrated circuit chip package 28 disposed on the bottom surface 18 and electrically connected to the flex pads 25 of the second set). Thus, when the chip stack 10 is mounted or electrically connected to an underlying component such as a printed circuit board (PCB) through the use of the leads 26 thereof, a slight gap is defined between the top surface 32 of the lowermost integrated circuit chip package 28 of the chip stack 10 and the printed circuit board 40.

**[0019]** Those of ordinary skill in the art will recognize that the number and orientation/pattern of leads 26 extending from the flex substrate 14 is dependent upon the desired "footprint" of the chip stack 10. In this regard, it is not necessary that the leads 26 protrude from each of the longitudinal and lateral peripheral edge segments 20, 22 of the flex substrate 14. For example, the leads 28 may extend from only each of the longitudinal peripheral edge segments 20, or each of the lateral peripheral edge segments 22. Additionally, the leads 26 may extend from one longitudinal peripheral edge segment 20 and/or one lateral peripheral edge segment 22. Moreover, the leads 26

need not necessarily be provided in a continuous row along any longitudinal or lateral peripheral edge segment 20, 22 of the flex substrate 14.

**[0020]** Referring now to Figure 3, there is shown a chip stack 100 which is constructed in accordance with a second embodiment of the present invention. The chip stack 100 comprises a flex circuit 112 which is identical to the flex circuit 12 of the chip stack 10 in almost all respects, except that the flex circuit 112 of the chip stack 100 does not include the second set of flex pads 25 described above. Thus, the first conductive pattern of the flex circuit 112 comprises only the first set of flex pads 224 disposed in a generally rectangular pattern or array in the central portion of the top surface 116 of the flex substrate 114. In the flex circuit 112, the leads 126 thereof are electrically connected to respective ones of the flex pads 224 of the first set via conductive traces which extend within the flex substrate 114. It is contemplated that the conductive traces may be arranged in a pattern such that two or more of the flex pads 224 of the first set may be electrically connected to a single lead 126.

**[0021]** The chip stack 100 of the second embodiment further comprises two identically configured integrated circuit chip packages 128 which are identical to the integrated circuit chip packages 28 of the chip stack 10, and each preferably comprises a rectangularly configured package body 130 having a plurality of conductive contacts 136 disposed on the bottom surface 134 thereof. Like the integrated circuit chip packages 28, each of the integrated circuit chip packages 128 preferably comprises a CSP device such as a BGA device, a fine pitch BGA device, or a flip chip device.

**[0022]** In the chip stack 100 of the second embodiment, one of the integrated circuit chip packages 128 is

electrically connected to the first conductive pattern of the flex circuit 112. More particularly, the conductive contacts 136 of one of the integrated circuit chip packages 128 are electrically connected to respective ones of the flex pads 224 of the first set. The conductive contacts 136 and flex pads 124 are preferably arranged in identical patterns. The remaining integrated circuit chip package 128 in the chip stack 100 (i.e., the lowermost integrated circuit chip package 128 in the chip stack 100) is attached to the bottom surface 118 of the flex substrate 114 of the flex circuit 112. More particularly, the top surface 132 of the package body 130 of the lowermost integrated circuit chip package 128 is rigidly affixed to the bottom surface 118 via an adhesive layer 142. As seen in Figure 3, the leads 126 of the flex circuit 112 and integrated circuit chip packages 128 are preferably sized relative to each other such that the outwardly turned distal ends of the leads 126 and the conductive contacts 136 of the lowermost integrated circuit chip package 128 (which is adhesively affixed to the bottom surface 118 of the flex substrate 114) extend in substantially co-planar relation to each other. Thus, in the chip stack 100 of the second embodiment, the leads 126 and conductive contacts 136 collectively define a composite footprint (ball and lead) for the chip stack 100 which is electrically connectable to an underlying component such as a printed circuit board 140.

**[0023]** The chip stack 100 of the second embodiment is preferably assembled by initially electrically connecting one of the integrated circuit chip packages 128 to the first conductive pattern of the flex circuit 112 in the above-described manner. Thereafter, the remaining integrated circuit chip package 128 is secured to the bottom surface 118 of the flex substrate 114 in the above-

described manner. Those of ordinary skill in the art will recognize that an assembly sequence varying from that described above may be employed for use in relation to the chip stack 100 of the second embodiment. Additionally, if desired, a layer 138 of flux/underfill material may be applied between the bottom surface 134 of the uppermost integrated circuit chip package 128 and the top surface 116 of the flex substrate 114 of the flex circuit 112.

**[0024]** Referring now to Figure 4, there is depicted a chip stack 200 constructed in accordance with a third embodiment of the present invention. The chip stack 200 of the third embodiment is virtually identical to the chip stack 100 of the second embodiment, with the exception that the leads 238 of the flex circuit 212 of the chip stack 200, each comprise a J-lead having a generally J shape as opposed to the S-leads shown and described in relation to the flex circuit 112. In the chip stack 200, the leads 238 and integrated circuit chip packages 228 are sized and configured relative to each other such that the inwardly turned distal ends of the leads 238 and the conductive contacts 236 of the lowermost integrated circuit chip package 228 extend in substantially co-planar relation to each other so as to collectively define a composite footprint (ball and lead) for the chip stack 200 which is electrically connectable to an underlying component such as a printed circuit board 240.

**[0025]** Those of ordinary skill in the art will recognize that, though not shown, each of the leads 26 of the chip stack 10 may alternatively be configured as a J-lead as opposed to an S-lead. Additionally, the leads 26 of the chip stack 10, as well as the leads 126 of the chip stack 100, may alternatively be configured as gull-wing leads as opposed to S-leads. It is contemplated that in each embodiment of the present chip stack, the flex circuit will

initially be formed such that a plurality of metal tabs extend linearly from the longitudinal peripheral edge segment(s) and/or lateral peripheral edge segment(s) thereof. Subsequent to the electrical connection/adhesive attachment of the integrated circuit chip packages to the flex circuit, these linearly extending metal tabs can be bent or otherwise formed into the leads. As indicated above, the leads of any embodiment of the chip stack of the present invention may be formed into a J, S, or gull-wing shape.

**[0026]** Additional modifications and improvements of the present invention may also be apparent to those of ordinary skill in the art. Thus, the particular combination of parts described and illustrated herein is intended to represent only certain embodiments of the present invention, and is not intended to serve as limitations of alternative devices within the spirit and scope of the invention.